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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known

Application Number 10/811726

Filing Date

First Named Inventor	Ravishankar Sundaresan
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Art Unit

Examiner Name _____

Attorney Docket Number	91-C-134D2 (STMI01-00098)
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Sheet	1	of	3
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)	MM-DD-YYYY			
JA	AF	JP 7132365	08/16/1982		—	
JA	AG	JP 3-260162	10/27/1988	NEC Corp	—	
JA	AH	JP 1-179367	07/17/1989	NEC Corp	—	
JA	AI	JP 1-214172	08/28/1989	Nippon Teleg.	—	
JA	AJ	JP 1-260857	10/18/1989	OkI Electric	—	
JA	AK	JP 2-23669	01/25/1990	Seiko Epson	—	

**Examiner
Signature**

Date
Considered

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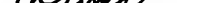
(Use as many sheets as necessary)

Complete if Known

Application Number	10/811 729
Filing Date	
First Named Inventor	Ravishankar Sundares
Art Unit	
Examiner Name	
Attorney Docket Number	91-C-134D2 (STM101-0

Sheet	2	of	3
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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ^o
		Country Code ³ * Number ⁴ * Kind Code ⁵ (if known)				
JK	BA	JP 2-197173	08/03/1990	Fujitsu Ltd.		
JK	BB	JP 2-99478	04/05/1990	Toshiba Corp.		
JK	BC	EP 0 457 434 A1	11/21/1991	Sharp Kabushiki		

Examiner Signature		Date Considered	10/12/04
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		Application Number	10/811729		
		Filing Date			
		First Named Inventor	Ravishankar Sundares		
		Art Unit			
		Examiner Name			
Sheet	3	of	3	Attorney Docket Number	91-C-134D2 (STMI01-0)

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JK	CA	OHKUBO, et al., "16Mbit SRAM Cell Technologies for 2.0V Operation," 1991 IEEE, IEDM, pp. 91-481 - 91-484.	
JK	CB	LIU, et al., "Inverted Thin-Film Transistors with a Simple Self-Aligned Lightly Doped Drain Structure," IEEE Transactions on Electron Devices, Vol. 39, No. 12, December 1992.	
JK	CC	LIU, et al., "High Reliability and High Performance 0.35 μ m Gate-Inverted TFT's for 16Mbit SRAM Applications Using Self-Aligned LDD Structures," 1992 IEEE, IEDM 92-823 - 92-826	
JK	CD	FURUTA, et al., "Hot-Carrier Induced Ion/Ioff Improvement of Offset PMOS TFT," 1991 Symposium on VLSI Technology, Digest of Technical Papers, IEEE Cat. No. 91, Ch. 3017-1, pp. 27-28	
JK	CE	FICHTNER, W. et al., "Experimental Results on Submicron-Size p-Channel MOSFET's," IEEE Electron Device Letters, Vol. EDL-3, No. 2 (February 1982).	
JK	CF	Article entitled "A Polysilicon Transistor Technology for Large Capacity SRAMs" by S. Ikeda, et al., IEDM 90, pp. 469-472, 1990.	
JK	CG	Article entitled "A 5.9 m2 Super Low Power SRAM Cell Using a New Phase-Shift Lithography" by T. Yamanaka, et al., IEDM 90, pp. 477-480, 1990.	
JK	CH	HAYASHI, et al., "A High Performance Polysilicon TFT Using RTA and Plasma Hydrogenation Application to High Stable SRAMs of 16Mbit and Beyond," 1992 Symposium on VLSI Technology Digest of Technical Papers, 1992 IEEE, pp. 36-37	
JK	CI	WOLF, et al., Silicon Processing for the VLSI Era, Vol. 1 - Processing Technology, 1986, Lattice Press, pp. 308-309.	

Examiner Signature		Date Considered	10/16/04
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